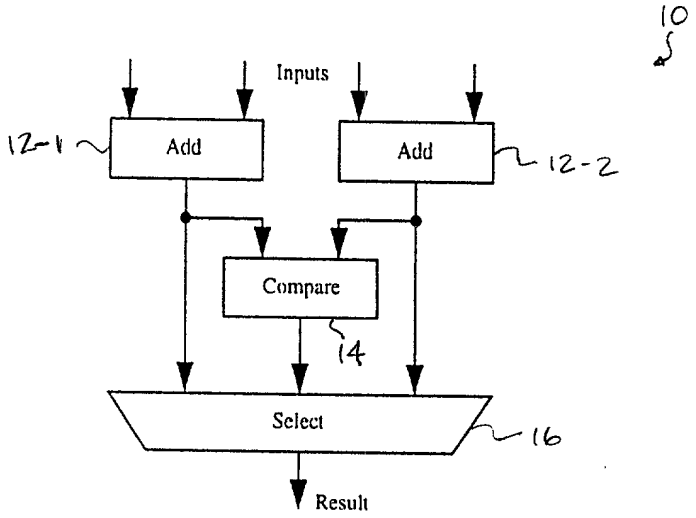
10
Inputs
12-1
Add
Add
12-2
Compare
14
Select
16
Result

FIG. 1

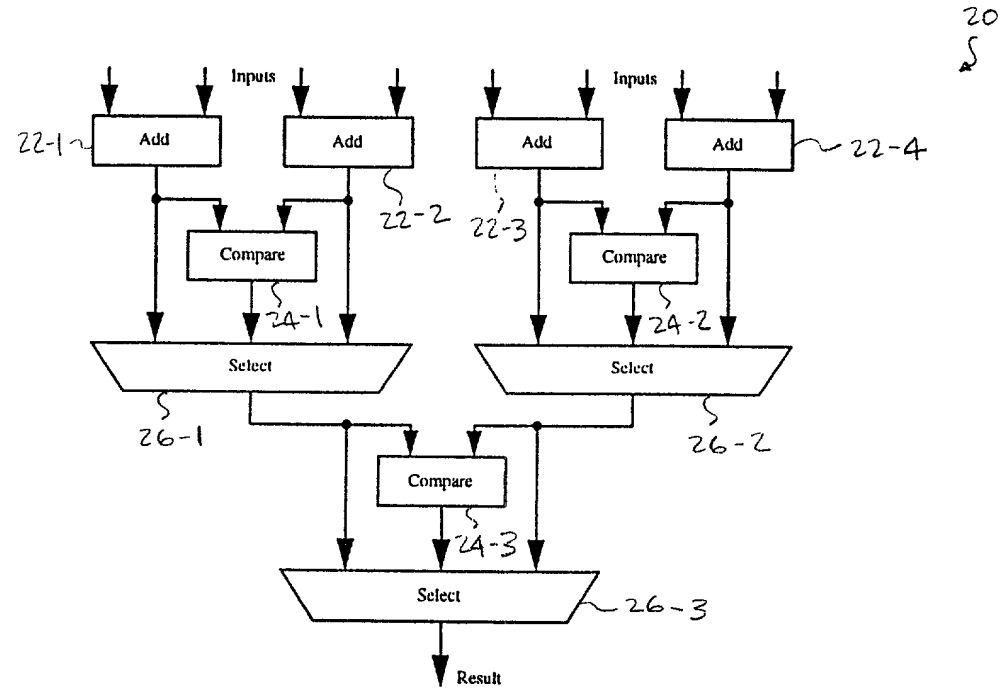
20
Inputs
Inputs
22-1
Add
Add
Add
Add
22-4
22-2
22-3
Compare
Compare
24-1
24-2
Select
Select
26-1
26-2
Compare
24-3
Select
26-3
Result

FIG. 2

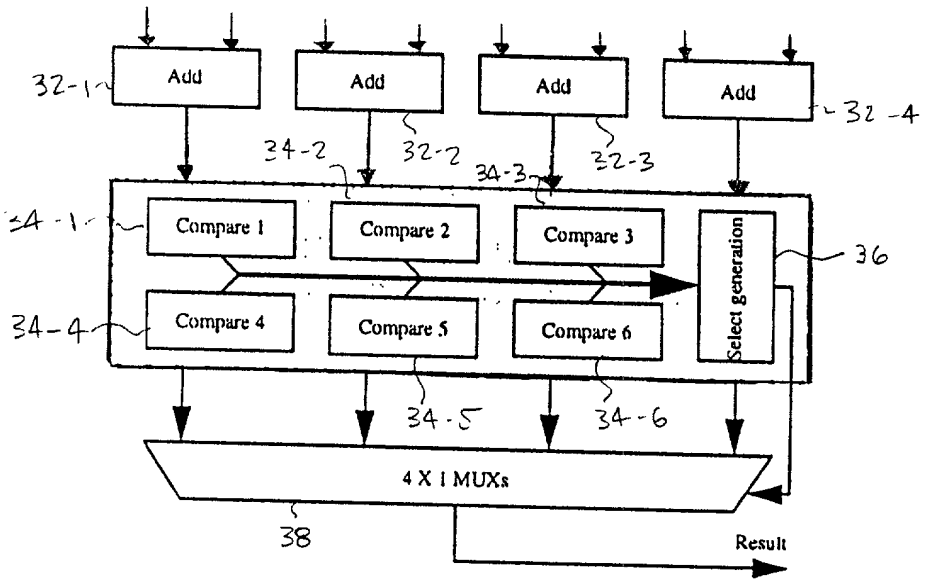
30
32-1
Add
Add
Add
Add
32-4
34-2
32-2
34-3
32-3
34-1
Compare 1
Compare 2
Compare 3
Select generation
36
34-4
Compare 4
Compare 5
Compare 6
34-5
34-6
4 X 1 MUXs
38
Result

FIG. 3

0	a7	a6	a5	a4	a3	a2	a1	a0	← a
0	b7	b6	b5	b4	b3	b2	b1	b0	← b
1	$\overline{c7}$	$\overline{c6}$	$\overline{c5}$	$\overline{c4}$	$\overline{c3}$	$\overline{c2}$	$\overline{c1}$	$\overline{c0}$	← $\overline{c}$
1	$\overline{d7}$	$\overline{d6}$	$\overline{d5}$	$\overline{d4}$	$\overline{d3}$	$\overline{d2}$	$\overline{d1}$	$\overline{d0}$	← $\overline{d}$
								1	← CORRECTION BIT

FIG. 4A

Cout(0)	Cout(1)	Remarks
0	0	$p < q$
0	1	$p = q \Rightarrow p - q = 0$
1	0	Impossible
1	1	$p > q$

FIG. 4B

	t7'	s7	s6	s5	s4	s3	s2	s1	
1	t7	t6	t5	t4	t3	t2	t1	t0	Ø

FIG. 4C

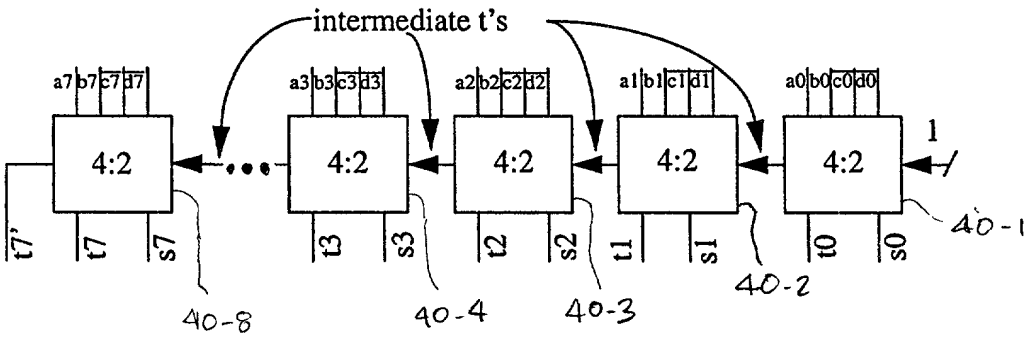
intermediate t's
a7 b7 c7 d7
a3 b3 c3 d3
a2 b2 c2 d2
a1 b1 c1 d1
a0 b0 c0 d0
4:2
4:2
4:2
4:2
4:2
1
t7'
t7
s7
t3
s3
t2
s2
t1
s1
t0
s0
40-8
40-4
40-3
40-2
40-1

FIG. 4D

40-n

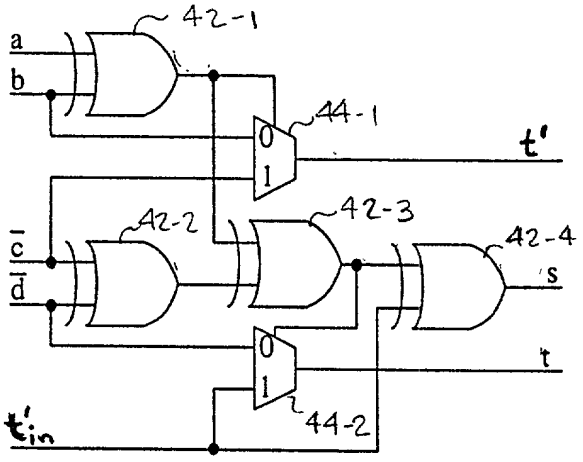

FIG. 4E

Input a		1	1	0	0	0	1	1	0
Input b		0	0	1	1	1	0	0	1
Input c		1	1	1	1	0	0	0	0
Input d		0	0	0	0	1	0	0	0
The next 4 rows represent the inputs of 4:2 compression logic, analogous to that represented by Figure 4A									
Input a	0	1	1	0	0	0	1	1	0
Input b	0	0	0	1	1	1	0	0	1
Input $\bar{c}$	1	0	0	0	0	1	1	1	1
Input $\bar{d}$	1	1	1	1	1	0	1	1	1
Correction bit									1
t' bits (shaded bits are internal to the network of 4:2 compressors, the unshaded bit is t7')	0	0	0	0	1	1	1	1	1
s bits		0	0	0	1	1	0	0	0
t bits	1	1	1	1	0	1	1	1	
Output of 4:2 compression network; s, t bit vectors: carry output from the MSB indicates the relative magnitudes of a + b and c + d. In this case, Cout = 1 which implies a + b > c + d	0	0	0	0	1	1	0	0	ϕ
	1	1	1	1	0	1	1	1	

FIG. 4F

Input a		1	1	0	0	0	1	1	0
Input b		0	0	1	1	1	0	0	1
Input c		1	1	1	1	0	0	0	0
Input d		0	0	0	0	1	1	1	1
The next 4 rows represent the inputs of 4:2 compression logic, analogous to that represented by Figure 4A									
Input a	0	1	1	0	0	0	1	1	0
Input b	0	0	0	1	1	1	0	0	1
Input $\bar{c}$	1	0	0	0	0	1	1	1	1
Input $\bar{d}$	1	1	1	1	1	0	0	0	0
Correction bit									1
t' bits (shaded bits are internal to the network of 4:2 compressors, the unshaded bit is t7')	0	0	0	0	1	1	1	1	1
s bits		0	0	0	1	1	1	1	1
t bits	1	1	1	1	0	0	0	0	
Output of 4:2 compression network; s, t bit vectors: carry output from the MSB indicates the relative magnitudes of a + b and c + d. In this case, Cout = 0 which implies a + b ≤ c + d (Conditional carries Cout(0) = 0 and cout(1) = 1 in this case)	0	0	0	0	1	1	1	1	ϕ
	1	1	1	1	0	0	0	0	

FIG. 4G

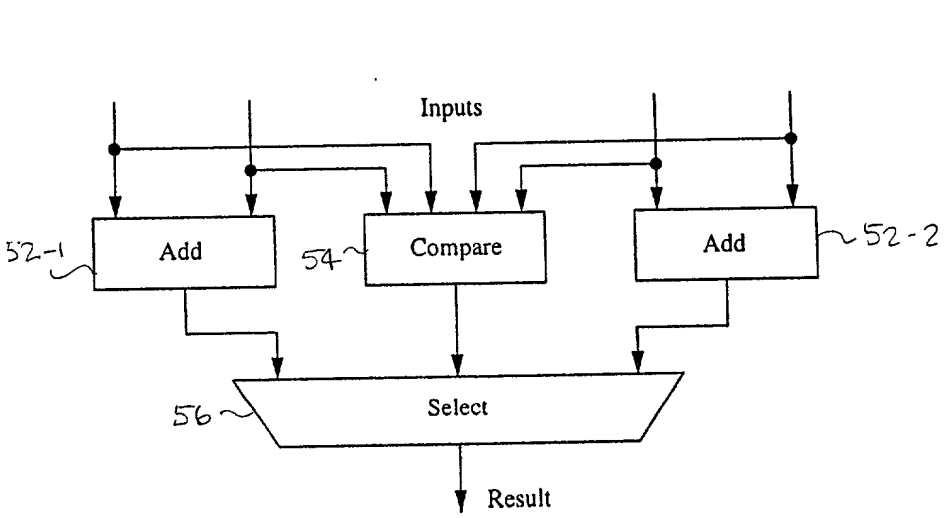
50
Inputs
52-1
Add
54
Compare
Add
52-2
56
Select
Result

FIG. 5

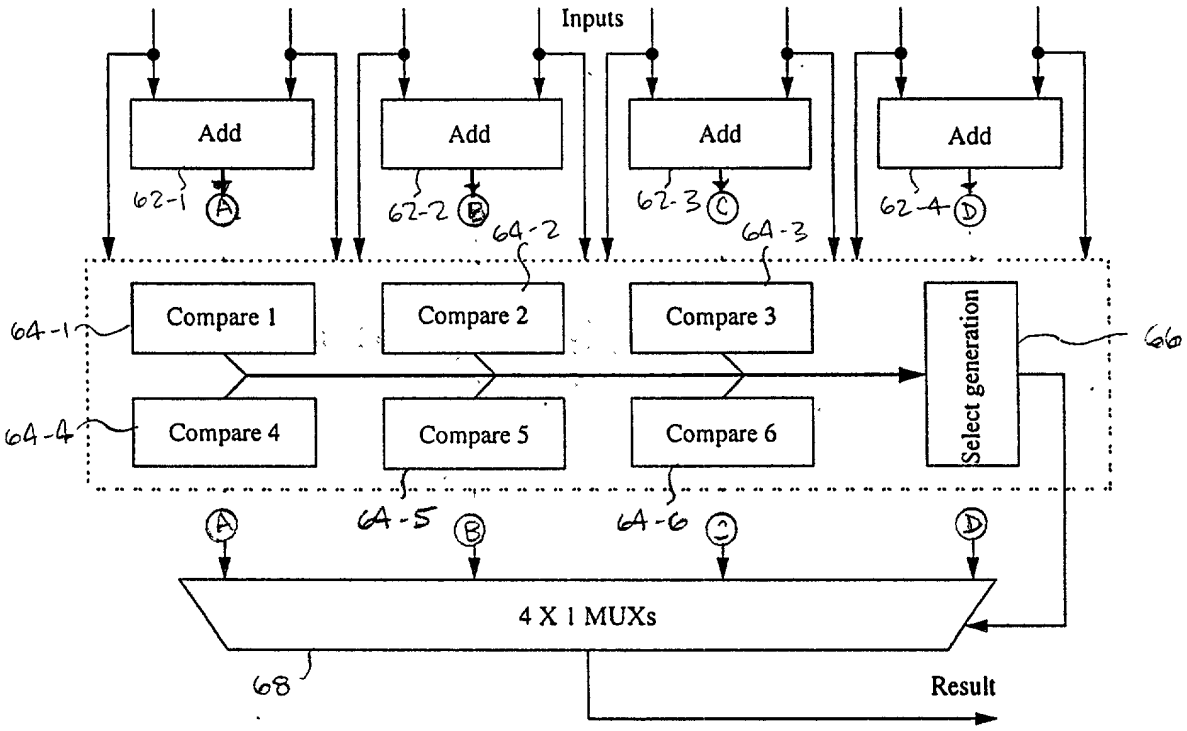
60
Inputs
Add
Add
Add
Add
62-1
A
62-2
B
62-3
C
62-4
D
64-2
64-3
64-1
Compare 1
Compare 2
Compare 3
Select generation
66
64-4
Compare 4
Compare 5
Compare 6
64-5
64-6
4 X 1 MUXs
68
Result

FIG. 6

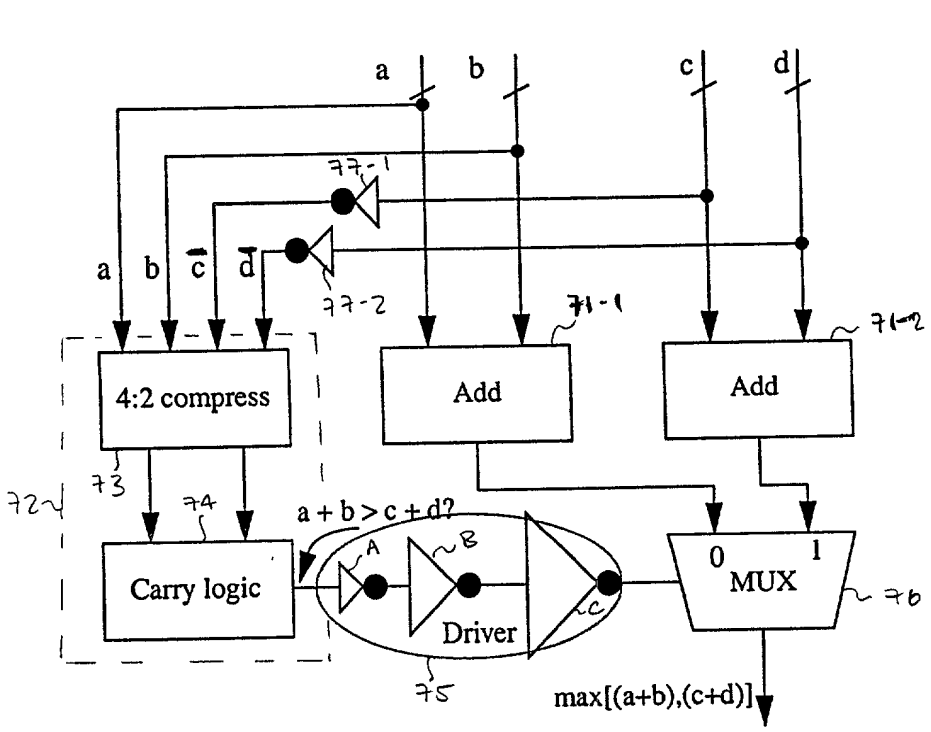
70
a
b
c
d
77-1
77-2
a
b
c̄
d̄
71-1
71-2
4:2 compress
Add
Add
73
72
74
a + b > c + d?
A
B
Carry logic
Driver
C
0
1
MUX
76
75
max[(a+b),(c+d)]

FIG. 7A

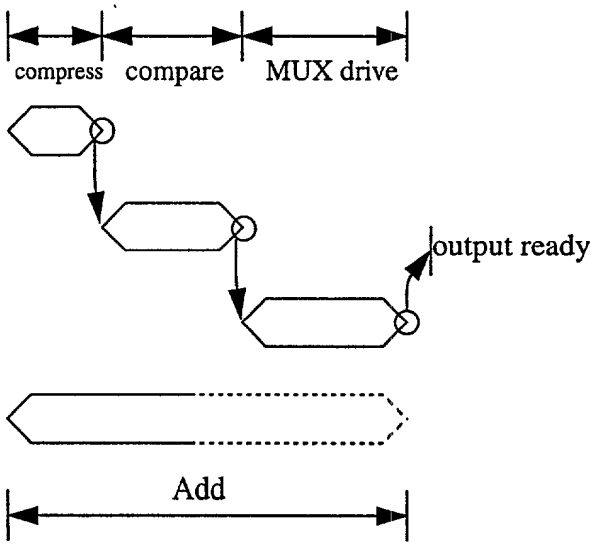
compress
compare
MUX drive
output ready
Add

FIG. 7B

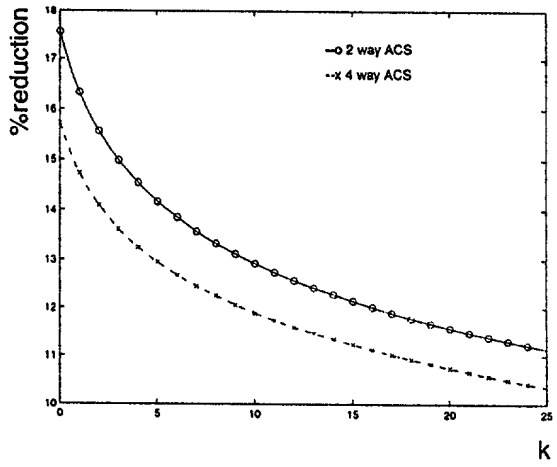
%reduction
k
o 2 way ACS
x 4 way ACS
18
17
16
15
14
13
12
11
10
0
5
10
15
20
25

FIG. 8

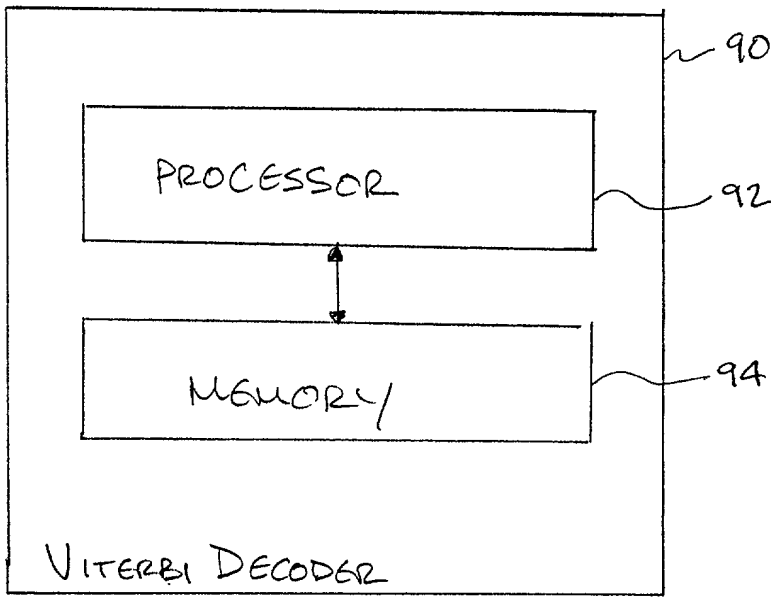

FIG. 9